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1 [Translating discrete-time simulink to lustre](#)



Stavros Tripakis, Christos Sofronis, Paul Caspi, Adrian Curic
 November 2005 ACM Transactions on Embedded Computing Systems (TECS),
 Volume 4 Issue 4

Publisher: ACM

Full text available: [pdf\(827.48 KB\)](#)

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We present a method of translating discrete-time Simulink models to Lustre programs. Our method consists of three steps: type inference, clock inference, and hierarchical bottom-up translation. In the process, we explain and formalize the typing and ...

Keywords: Code generation, Lustre, Simulink, embedded software

2 [Efficient power co-estimation techniques for system-on-chip design](#)



Marcello Lajolo, Anand Raghunathan, Sujit Dey

January DATE '00: Proceedings of the conference on Design, automation and test in Europe

Publisher: ACM

Full text available: [pdf\(124.92 KB\)](#) [Publisher](#)

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3 [A 90nm low-power FPGA for battery-powered applications](#)



Tim Tuan, Sean Kao, Arif Rahman, Satyaki Das, Steve Trimberger

February FPGA '06: Proceedings of the 2006 ACM/SIGDA 14th international symposium on Field programmable gate arrays

Publisher: ACM

Full text available: [pdf\(233.96 KB\)](#)

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Programmable logic devices such as FPGAs are useful for a wide range of applications. However, FPGAs are not commonly used in battery-powered applications because they consume more power than ASICs and lack power management features. In this paper, we ...

Keyw ords: FPGAs, field-programmable gate arrays, low-power design, programmable logic

4 [Functional verification of task partitioning for multiprocessor embedded systems](#)



Dipankar Das, P. P. Chakrabarti, Rajeev Kumar

September ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 12 Issue 4

Publisher: ACM

Full text available: [pdf\(533.81 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

With the advent of multiprocessor embedded platforms, application partitioning and mapping have gained primacy as a design step. The output of this design step is a multithreaded partitioned application where each thread is mapped to a processing element ...

Keyw ords: Containment checking, UML activity diagrams, multiprocessor embedded systems, state space reduction

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